

ABSTRACT OF THE DISCLOSURE

A phase-locked loop circuit has a DLL circuit in a stage preceding an analog PLL circuit. The DLL circuit detects a phase difference between a reference clock signal and a feedback signal, changes the detected phase difference to a phase difference increased so as to be greater than a steady state phase error which the analog PLL circuit has, and supplies the resultant phase difference to the analog PLL circuit. While the phase difference between the reference clock signal and the feedback signal is being detected by the DLL circuit, the analog PLL circuit operates to reduce the increased phase difference to the steady state phase error. As a result, the phase difference between the reference clock signal and the feedback signal is reduced to a sensitivity limit of a phase comparator in the DLL circuit.